UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/825,357	04/16/2004	Dai Yun Lee	8733.1031.00-US	8106

30827 7590 12/10/2008

MCKENNA LONG & ALDRIDGE LLP
1900 K STREET, NW
WASHINGTON, DC 20006

EXAMINER	
LAM, VINH TANG	
ART UNIT	PAPER NUMBER
2629	
MAIL DATE	DELIVERY MODE
12/10/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/825,357	LEE ET AL.	
	Examiner	Art Unit	
	VINH T. LAM	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 May 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) *6* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 7-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Claim **6** is withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected Species **I** there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 05/07/2008.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims **1-5**, **7-10**, and **19-25** are rejected under 35 U.S.C. 102(b) as being anticipated by **Inukai (US Patent Application 2002/0000576).**

Regarding Claim **1**, **Inukai** teaches an electro-luminescence display device, comprising:

a plurality of pixels arranged in a matrix type (Col. **4**, [**0075**], FIG. **2**);

a plurality of data lines for applying video signals to the pixels (Col. **4**, [**0074**], FIG. **2**); and

a plurality of gate lines crossing the data lines (Col. **4**, [**0074**], FIG. **2**), wherein each of the gate lines connected to the pixels positioned adjacently to each other at the upper and lower sides of the gate line (Col. **4**, [**0078**] - [**0080**], FIG. **3**).

Regarding Claim **19**, **Inukai** teaches an electro-luminescence display device, comprising:

a plurality of pixels arranged in a matrix type (Col. **4**, [**0075**], FIG. **2**);

a plurality of data lines for applying video signals to the pixels (Col. **4**, [**0074**], FIG. **2**);

a plurality of gate lines crossing the data lines (Col. **4**, [**0074**], FIG. **2**), wherein each of the gate lines is shared with the pixels positioned adjacently to each other at the upper and lower sides of the gate line(Col. **4**, [**0078**] - [**0080**], FIG. **3**); electro-luminescence cells provided for each pixel (Col. **4**, [**0075**], FIG. **3**);

a supply voltage line for supplying a driving voltage to the electro-luminescence cells (Col. **4**, [**0077**], FIG. **3**);

driving circuits for applying a current corresponding to the video signals to the electro-luminescence cells in response to the video signals (Col. **4**, [**0079**] - [**0080**], FIG. **3**); and

control circuits connected to the data lines to apply the video signals supplied to the data lines to the driving circuits (Col. **4**, [**0078**], FIG. **3**).

Regarding Claims **2** and **20**, **Inukai** teaches the electro-luminescence display device according to claims 1 and 19, further comprising:

a gate driver for applying a gate signal having a turn-on potential during two horizontal periods to the gate lines (Col. **7**, [**0124**], [**0125**], FIG. **5A**).

Regarding Claims **3** and **21**, **Inukai** teaches the electro-luminescence display device according to claims 2 and 20, wherein a gate signal applied to the ith

gate line (wherein i is an integer) overlaps a gate signal applied to the (i+1)th gate line during one horizontal period (Col. **7**, [**0124**], [**0125**], FIG. **5A**).

Regarding Claim **4**, **Inukai** teaches an electro-luminescence display device, comprising:

electro-luminescence cells arranged in a matrix type (Col. **4**, [**0075**], FIG. **2**) at crossings of gate lines and data lines (Col. **4**, [**0074**], FIG. **2**);

a supply voltage line for supplying a driving voltage to the electro-luminescence cells (Col. **4**, [**0077**], FIG. **3**);

driving circuits for controlling a current applied from the driving voltage of the supply voltage line to the electro-luminescence cells in response to video signals, wherein each of the driving circuits includes a first driving circuit and a second driving circuit (Col. **4**, [**0079**] - [**0080**], FIG. **3**); and

control circuits for applying the video signals to the driving circuits, wherein the control circuits are positioned between the first driving circuit and the second driving circuit (Col. **4**, [**0078**], FIG. **3**).

Regarding Claims **5** and **22**, **Inukai** teaches the electro-luminescence display device according to claims 4 and 21, wherein

the first driving circuit provided at the ith horizontal line (wherein i is an integer) to apply the current to the electro-luminescence cell positioned at the ith horizontal line, in response to a video signal from the control circuit controlled by the ith gate line, when a gate signal is applied to the (i-1)th gate line (Col. **4**, [**0080**], FIG. **3**); and

the second driving circuit is provided at the (i+1)th horizontal line to apply the current to the electro-luminescence cell positioned at the (i+1)th horizontal line, in response to a video signal from the control circuit controlled by the ith gate line, when a gate signal is applied to the (i+1)th gate line (Col. **4**, [**0079**], FIG. **3**).

Regarding Claim **7**, **Inukai** teaches the electro-luminescence display device according to claim 5, wherein the (i+1)th gate line is connected to a driving circuit provided at the (i+2)th horizontal line (FIG. **2**).

Regarding Claim **8**, **Inukai** teaches the electro-luminescence display device according to claim 5, wherein the (i-1)th gate line is connected to a driving circuit provided at the (i-1)th horizontal line (FIG. **2**).

Regarding Claim **9**, **Inukai** teaches the electro-luminescence display device according to claim 5, wherein the first driving circuits includes

a first driving thin film transistor having a source terminal connected to the supply voltage line and a drain terminal connected to the electro-luminescence cell positioned at the ith horizontal line (Col. **4**, [**0082**], FIG. **3**);

a second driving thin film transistor having a drain terminal connected to a gate terminal of the first driving thin film transistor, a source terminal connected to the control circuit and a gate terminal connected to the (i-1)th gate line (Col. **4**, [**0080**], FIG. **3**); and

a storage capacitor connected between the source terminal and the gate terminal of the first driving thin film transistor (Col. **4**, [**0081**], FIG. **3**).

Regarding Claim **10**, **Inukai** teaches the electro-luminescence display device according to claim 5, wherein the second driving circuits includes:

a first driving thin film transistor having a source terminal connected to the supply voltage line and a drain terminal connected to the electro-luminescence cell positioned at the (i+1)th horizontal line (Col. **4**, **[0082]**, FIG. **3**);

a second driving thin film transistor having a drain terminal connected to a gate terminal of the first driving thin film transistor, a source terminal connected to the control circuit and a gate terminal connected to the (i+1)th gate line (Col. **4**, [**0080**], FIG. **3**); and

a storage capacitor connected between the source terminal and the gate terminal of the first driving thin film transistor (Col. **4**, **[0081]**, FIG. **3**).

Regarding Claim **23**, the electro-luminescence display device according to claim 22, wherein **Inukai** teaches one of the control circuits is positioned between the first driving circuit and the second driving circuit (Col. **4**, **[0078]**, FIG. **3**).

Regarding Claim **24**, **Inukai** teaches a method of driving an electro-luminescence display device, comprising: applying a gate signal having a turn-on potential during two horizontal periods to gate lines, wherein the gate signal applied to the ith gate line (wherein i is an integer) overlaps the gate signal applied to the (i-1)th gate line during one horizontal period (Col. **7**, **[0124]**, **[0125]**, FIG. **5A**).

Regarding Claim **25**, **Inukai** teaches the method according to claim 24, wherein a current corresponding to a video signal is applied to an electro-luminescence cell provided at the ith horizontal line during the one horizontal period in which the gate signal applied to the (i-1)th gate line overlaps the gate signal applied to the ith gate line (Col. **7**, [**0124**], [**0125**], FIG. **5A**).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims **11-18** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Inukai (US Patent Application 2002/0000576)** in view of **Komiya (US Patent No. 6924602).**

Regarding Claim **11**, **Inukai** teaches the electro-luminescence display device according to claim 9 or 10.

However, **Inukai** does not teach the control circuit includes the first and second control TFTs and their connections.

In the same field of endeavor, **Komiya** teaches the control circuit includes:

a first control thin film transistor having a source terminal connected to the supply voltage line and a drain terminal and a gate terminal connected to the source terminal of the second driving thin film transistor (Col. **3**, Ln. **34-44**, FIG. **1**); and

a second control thin film transistor having a drain terminal connected to the gate terminal of the first control thin film transistor, a source terminal connected to the data line and a gate terminal connected to the ith gate line (Col. **3**, Ln. **34-44**, FIG. **1**). for the benefit of reducing the aperture ratio by having an electro-luminescence display device with first and second driving circuits including thin film transistors, storage capacitors

and first and second driving circuits including thin film transistors for selectively controlling the respective driving circuits.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine **Inukai** teaching of the first and second driving circuits comprising thin film transistors and storage capacitors with **Komiya** teaching of control circuits having the first and second control thin film transistors in order to benefit of reducing the aperture ratio by having an electro-luminescence display device with first and second driving circuits including thin film transistors, storage capacitors and first and second driving circuits including thin film transistors for selectively controlling the respective driving circuits.

Regarding Claim **12**, the electro-luminescence display device according to claim 11, wherein **Inukai** teaches any one of the first and second control thin film transistors is provided at the ith horizontal line while the remaining control thin film transistor is provided at the (i+1) the horizontal line (Col. **4**, [**0079**], [**0080**], FIG. **3**).

Regarding Claim **13**, the electro-luminescence display device according to claim 11, **Inukai** further teaches a gate driver for applying a gate signal having a turn-on potential during two horizontal periods to the gate lines (Col. **7**, [**0124**], [**0125**], FIG. **5A**).

Regarding Claim **14**, the electro-luminescence display device according to claim 13, wherein **Inukai** teaches a gate signal applied to the ith gate line overlaps a gate signal applied to the (i+1)th gate line during one horizontal period (Col. **7**, [**0124**], [**0125**], FIG. **5A**).

Regarding Claim **15**, the electro-luminescence display device according to claim 13, wherein **Inukai** teaches,

if a gate signal is applied to the (i-1)th and ith gate lines, then the second driving thin film transistor connected to the (i-1)th gate line and the second control thin film transistor connected to the ith gate line are turned on (Col. **4**, [**0079**], [**0080**], FIG. **3**); and

as the second control thin film transistor is turned on, a video signal from the data line is applied to the first driving thin film transistor and the first control thin film transistor that are positioned at the ith horizontal line (Col. **4**, [**0079**], [**0080**], FIG. **3**).

Regarding Claim **16**, the electro-luminescence display device according to claim 15, wherein **Inukai** teaches the first driving thin film transistor positioned at the ith horizontal line applies the current corresponding to the video signal to the electro-luminescence cell provided at the ith horizontal line (Col. **4**, [**0084**], FIG. **3**).

Regarding Claim **17**, the electro-luminescence display device according to claim 15, wherein **Inukai** teaches the first control thin film transistor applies the current corresponding to the video signal from the supply voltage line to the data line (Col. **4**, [**0084**], FIG. **3**).

Regarding Claim **18**, the electro-luminescence display device according to claim 17, wherein **Inukai** teaches a voltage corresponding to the current flowing in the first control thin film transistor is stored in the storage capacitor (Col. **4**, [**0081**], FIG. **3**).

Conclusion

The prior arts made of record and not relied upon is considered pertinent to applicant's disclosure are: Moon (US Patent Application 2004/0189584) and Tanada (US Patent No. 6909409).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to VINH T. LAM whose telephone number is (571)270-3704. The examiner can normally be reached on M-F (7:30-5:00) EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on 571 272 1206. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/VTL/

/Amare Mengistu/
Supervisory Patent Examiner, Art Unit 2629